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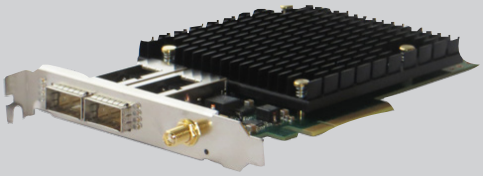

fbC8XG supporting the fbCapture framework

The Fiberblaze fbC8XG Card with fbCAPTURE API is a high port density packet capture and processing PCIe device. It performs at full line rate with zero packet loss on all eight 10GE ports with a wide variety of functions. The card's high port density is ideal for the data capture, processing, inline applications and special purpose function of fbCAPTURE.

With the high port density, it imbues applications with unprecedented scalability by offering traffic load balancing using the Tx channels of the ports. In a simple star architecture it can load balancing across 8 additional external processing appliances, as well as via DMA to the card's host appliance itself.

Based on powerful FPGA Hardware technology, fbC8XG is a high performance OEM hardware platform intended for 10GE interfacing. Via its dual QSFP+ slots fitted with fanout modules it exposes all eight bidirectional 10GE interfaces of the QSFP+ ports. With its PCIe Gen3 support, it features unrivaled performance in transfers to and from host systems.

NETWORK INTERFACE
- IEEE standard: IEEE 802.3 10 Gbit/s Ethernet
- Physical interface: 2 x QSFP+ ports
- Data rate: 8 x 10 Gbit/s
- Supported QSFP+ modules with 4x10GE fan-out:
  - 4-channel 10GBASE-SR fan-out
  - 4-channel 10GBASE-LR fan-out
  - QSFP+ Fanout to 4 x 10G SFP+ DAC
- Ethernet PHY directly embedded in FPGA for full packet control
- Daisy chain between multiple cards supported

HOST INTERFACE
- Physical bus connector: 8-lane PCIe
- PCIe bus type: 1-8 lane PCIe Gen1/Gen2/Gen3
- PCIe compliant
- 64 logical channels that can be connected to DMA or egressed via physical Tx ports

ON BOARD MEMORY
- 8 GB (2x4GB 64 bit DDR3)

PERFORMANCE
- Capture rate (card internal): Full line rate
- Capture rate (bursts): Full line rate
- Capture rate (sustained): 55 Gbps
- Transmission rate (inline host DMA): 40 Gbps
- Transmission rate (inline bypass): 68 Gbps
- Transmission rate (daisy chain): Full line rate

LATENCY
- Less than 3 µs to host memory
- Less than 3 µs from host memory to Tx

LATENCY (continued)
- Non-blocking sending, allowing user applications to operate independently

TIME STAMPING AND SYNC
- Resolution = 3.2 ns
- Accuracy down to 20 ns
- Optional external synchronization via PPS
- Customization for PTP IEEE 1588-2008 RJ45
- Master/slave time sync between multiple cards

CONFIGURATION
- Dual boot images with automatic fallback to fail-safe image
- Full firmware upgrades via supplied tools or fbCAPTURE API

ENVIRONMENT
- Physical dimensions: half length, standard height
- PCIe: 111 x 169 mm
- Weight: 292g
- Operational power consumption: Less than 39W
- Operating temperature: 0 – 55°C, 30 – 130°F
- Operating humidity: 20 – 80%
- Hardware compliance: RoHS, CE
- Passive cooling (no on-board fan required)

ADDITIONAL BOARD SUPPORT
- fbCAPTURE API
- On-board temperature sensor
- Internal board multi-color status LED
- Link and Activity LED for each port

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Dedication to Performance

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The fbCAPTURE Framework

The fbCAPTURE framework is a combination of FPGA firmware and a software API in C that utilizes the full potential present in a range of FPGA based network interface cards from Fiberblaze. The fbCAPTURE Cards are designed with a combination of a powerful FPGA and large amounts of high speed onboard memory to ensure zero packet loss even at line rate performance. The fbCapture API is common for all the capture cards for 1GE, 10GE, 40GE and 100GE line rates. This simplifies system integration greatly, as support for multiple network rates can be achieved with the same integration efforts.

SOFTWARE API

- Same API for all Fiberblaze capture cards
- WinPCAP and LibPCAP compatibility
- C based API (DLL/Shared library)
- Linux, Windows & FreeBSD
- Multi Direct Memory Access streaming using to Packet Ring Buffers (PRB)
- Up to 64 channels to host controlled PRBs
- 255 channels for traffic redirection
- User error handlers
- No additional SW library dependencies

SERVER LOAD BALANCING

- Host server traffic load balancing supported
- Up to 64 channels to multiple host processes' memory
- Selective traffic redirection
- Load balancing to external hosts via optical Tx interfaces
- Dual level load balancing. Hosts & CPUs
- Copy same PDU to multiple channels
- Distribution without CPU overhead using 2, 3, 5 and N tuple hashing or filter rules

SUPPORTED HARDWARE

- Fiberblaze cards for 1, 10, 40 and 100 Gbit/s using pluggable transceiver modules (SFP, SFP+, QSFP+, CFP4, QSFP 28)
- Ethernet PHY embedded in FPGA for full packet control
- PCIe Gen1, Gen2 and Gen3 support for optimal host throughput
- Monitoring via SPAN port/optical splitters
- Ethernet auto-negotiation
- Limitless Daisy Chaining of monitored optical fibers between cards, at full signal strength, reducing number tapping of points
- Board to board interconnect for data merge and redirection

FILTERS

- A wide range of inline filters can be defined and combined in real-time to meet a variety of filtering requirements on a wide range of protocol header parameters
- On-the-fly reconfiguration of filters
- Filter types available include ranges, pattern match, fixed/dynamic offset and value, bit masks and value, true/false, not, hash values, compounds and more on e.g.:
- Link layer:
  ARP, Tunnels (L2TP), MAC, VLAN incl. Stacked VLAN, MPLS, etc.
- Internet layer:
  IPv4, Ipv6, ICMP, RIP, OSPF, ECN, etc.
- Transport layer:
  UDP, TCP, SCTP, etc.
- Application layer:
  HTTP, FTP, LDAP, POP, RTP, SIP, SMTP, Telnet, GTPv1, GTPv2, RNSAP and RANAP via SIGTRAN, GTP-U payload headers etc.
- Option to allow on-wire error packets through
- Optional on-wire error and undersized frames to processing

PACKET SLICING

- A wide range of slicing rules can be applied to conserve memory and storage by truncating packets
- Fixed length slicing
- Dynamic slicing where truncation may start from any specified header and include user definable number of bytes thereafter

PACKET DESCRIPTOR

- Captured packets can be enriched with descriptors generated by the adapter at line rate.
- PCAP Descriptor
- Standard Descriptor
- Multiple Extended Descriptor
- Multiple time formats supported

PACKET PROCESSING

- Host acceleration of protocol parsing
- Zero copy PDU handling
- Packet layers indexing of protocol layers
- No protocol parsing needed for access to individual layers
- Optional insertion of alignment ticks (packets) in host memory buffer every 100ms
- Optimized packet transfers for batch processing

DEDUPLICATION

- Removal of duplicated packets
- Configurable duplication detection parameters

IP DEFRAGMENTATION

- IP fragments are correlated on-the-fly and processed as the initial fragment of the original packet
- Correlated fragment handling ensures that all related fragments are delivered to same channel as specified for the complete original packet
- True representation of on-wire packets

NETWORK STATISTICS

- Elaborated subset of RFC2819 RMON1
- Statistics each second for each interface
- Counters for special purpose firmwares
- Network counters include: number of octets, CRC align errors, undersize packets, oversize packets incl. Jumbo frames, packet size distribution & more
- Provided via API or via supplied independent Fiberblaze application

ON BOARD SENSOR READINGS

- Temperature with preset minimum, maximum card operating temperature
- Optical signal level readings
- Link status
- Provided via API or via supplied independent Fiberblaze application